

Fabrication and Characterization of Carbon Nanofiber-Based Vertically Integrated Schottky Barrier Junction Diodes

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ABSTRACT

We report on the fabrication and electrical characterization of active nanoscale electronic devices using single vertically aligned carbon nanofibers (VACNFs). A rectifying behavior consistent with a 0.3 eV Schottky barrier was found. Experimental results indicate that a region of semiconducting SiC is formed directly beneath the VACNF during the growth process, creating the Schottky-barrier junction between this semiconductor material and the metallic carbon nanofibers.

The development of nanoscale electronic (nanoelectronic) devices has recently become one of the most active fields of research in the physical sciences.^{1–4} Numerous research groups have developed techniques that utilize carbon nanotubes and/or semiconductor nanowires to form logic devices from these nanoscale electronic components.^{2–4} The majority of these approaches involve dispersing ex-situ grown nanotubes or nanowires onto prefabricated electrode arrays or alignment mark patterns. More recently, the direct growth of nanotubes horizontally between two electrodes has been demonstrated.⁴

Vertically aligned carbon nanofibers (VACNFs) can be synthesized deterministically using catalytic dc plasma

enhanced chemical vapor deposition (DC-PECVD). By lithographically patterning the growth catalyst and controlling the growth process, excellent control over the location, geometry, and composition of the fibers can be achieved.^{4–9} This controlled synthesis capability has enabled the integration of individual carbon nanofibers into field emission electron sources, active electrochemical probes, and intracellular devices.^{4,10–12} In this work we demonstrate the fabrication of vertically integrated nanoelectronic devices based on single VACNFs that have been deterministically grown. These devices demonstrate robust and reproducible characteristics. The vertical orientation of these structures provides an opportunity to achieve higher levels of integration than that provided by nanoelectronic device structures limited to in-plane orientations.

A summary of the fabrication process is illustrated in Figure 1. N-type Si wafers with resistivity ranging from 1 to 10 Ω -cm were used as substrates. Electron-beam lithography was used to pattern catalyst sites for individual fiber growth and alignment marks for subsequent lithographic patterning. Following metallization and liftoff pattern transfer, the growth of VACNFs was performed at 700 °C from C₂H₂ and NH₃ precursors in a DC-PECVD chamber. The

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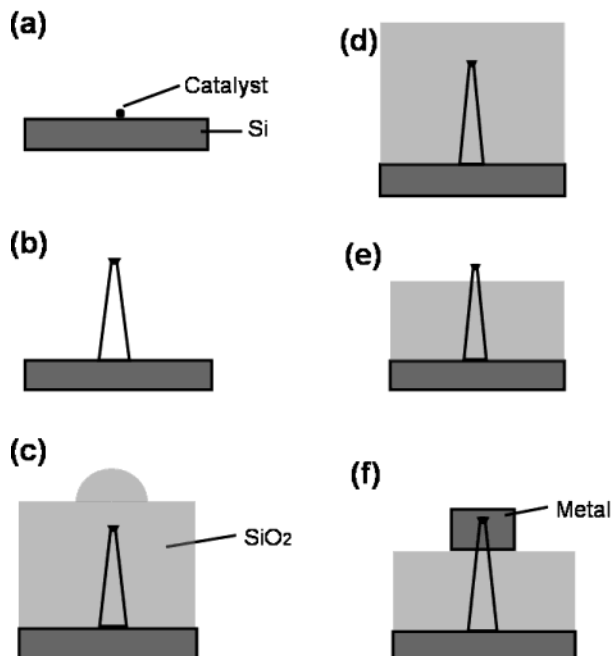


Figure 1. Summary of the device fabrication process: (a) definition of the VACNF growth sites; (b) VACNF growth; (c) deposition of conformal SiO₂ layer; (d) planarization by chemical mechanical polishing; (e) reactive ion etching to uncover the nanofiber tip; (f) metallization via physical vapor deposition.

details of the growth process have been described elsewhere.^{6,7,9,12} The VACNFs produced in this work were typically $\sim 1 \mu\text{m}$ tall with base diameters ranging from 200 to 300 nm and tip diameters ranging from 40 to 70 nm. An SEM image of an as-grown nanofiber is shown in Figure 2a taken at 30° from normal incidence.

After inspecting the fibers, the substrates with VACNFs were coated in a conformal layer of SiO₂ deposited in a silane-based rf PECVD process (Figure 1c). Chemical mechanical polishing (CMP) was then performed to planarize the surface of the substrates (Figure 1d), and this process was arrested before reaching the fiber tip. The tips were uncovered by reactive ion etching (RIE) using a CHF₃/O₂ plasma (Figure 1e). It was previously reported that these processes do not produce significant damage to the VACNF structure.⁶ Conventional photolithography was performed to produce interconnects to individual VACNF tips. This pattern was metallized with a 1000 Å layer of Ti followed by a 500 Å layer of Au using electron beam physical vapor deposition (PVD, Figure 1f). It has been shown that Ti thin films adhere to graphitic carbon better than many other metals.¹³ The relatively inert Au layer was chosen to protect the electrode surface from contamination.

An SEM image of the upper electrode of a completed device structure is shown in Figure 2b, taken at normal incidence to the sample. The bright portion of the image is the VACNF tip coated with the electrode metallization. An oblique angle tapping mode AFM image is shown in Figure 2c. The crater surrounding the tip is an artifact of the CMP process.

The DC current vs voltage (I - V) characteristics of the devices were investigated using the Si substrate as a bottom

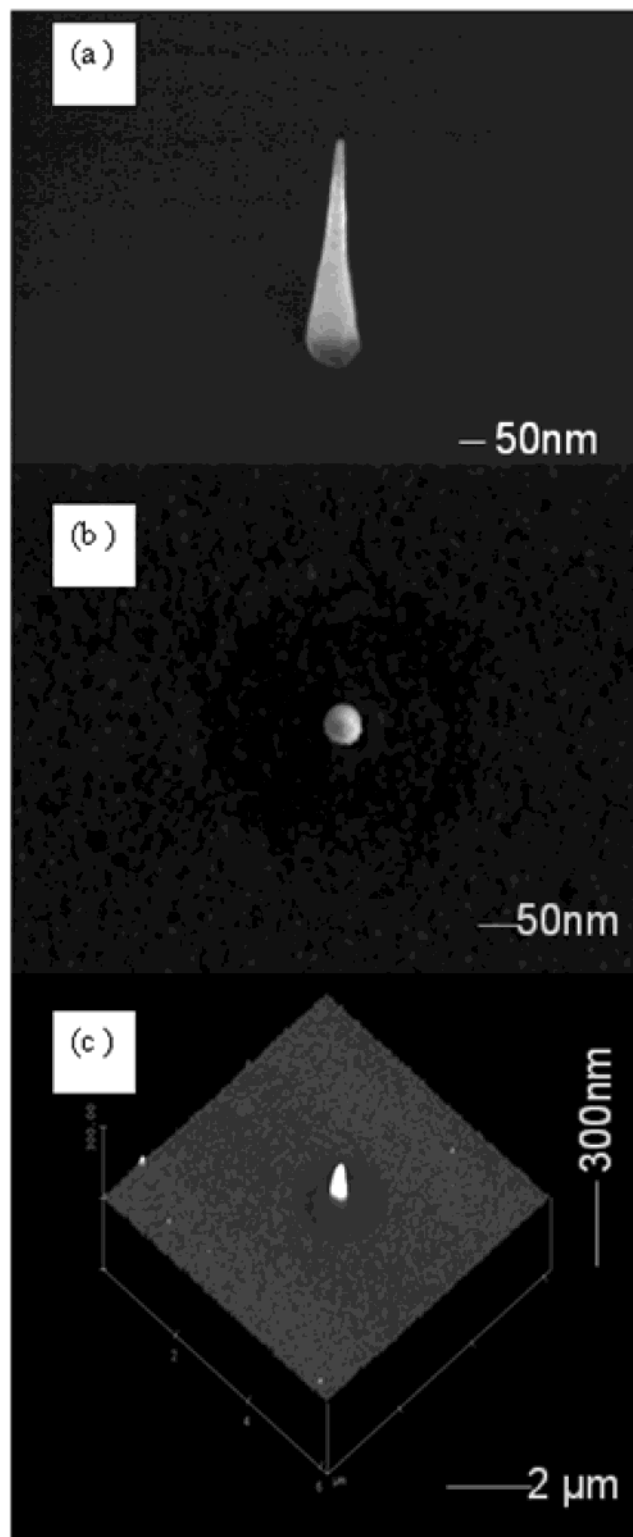


Figure 2. (a) SEM image of the as-grown nanofiber; (b) SEM image of a finished device; (c) AFM image of the finished device.

electrode. Each device was placed onto a variable temperature test fixture controlled by a Signatone model S-1060R temperature controller. This fixture was contained inside an enclosure designed to eliminate optical effects. All I - V data were obtained using a Hewlett-Packard 4156 source measure unit (SMU) system. The top electrode potential was swept from 0 to +5 V and from 0 to -5 V, with the Si substrate

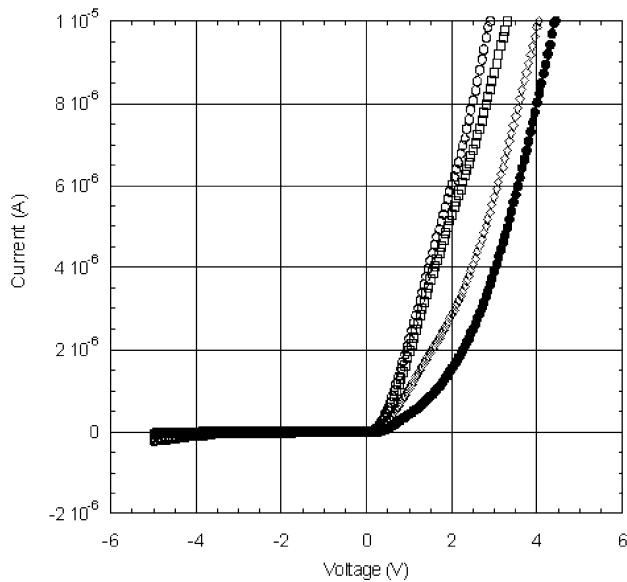


Figure 3. (a) Typical I – V characteristics of the devices of Figures 1 and 2 at four different temperatures. These measurements show rectifying behavior with a high reverse-breakdown voltage. The forward bias current increased with temperature, consistent with the Schottky barrier junction model. (○) 120 °C; (□) 90 °C; (◇) 60 °C; (●) 20 °C.

always at ground potential to reveal the rectifying behavior. I – V data was obtained at temperatures varying from 20 °C to 120 °C in 10 °C steps. A typical example of these results is shown in Figure 3 at four different temperatures.

Rectifying behavior was reproducibly observed for each device tested. A slight temperature dependence on the forward and reverse bias current was also observed. This behavior is consistent with the thermionic model of Schottky barrier junction (SBJ) diodes. In the ideal thermionic model, the I – V characteristics follow the relationship

$$I = I_{\text{sat}}[\exp(qV/kT) - 1] \quad (1)$$

where q is the electronic charge, V is the voltage across the junction, and I_{sat} is the reverse bias saturation current. I_{sat} is given by

$$I_{\text{sat}} = SAT^2 \exp(-q\phi_b/kT) \quad (2)$$

where S is the diode area, A is the Richardson constant, and ϕ_b is the effective barrier height at the junction. The I – V characteristics of devices often deviate from ideal SBJ behavior. In this case, the generalized diode equation can be applied:

$$I = I_{\text{sat}}[\exp(eV/nkT) - 1] \quad (3)$$

where n is known as the ideality factor. The value of n ranges between 1 and 2 with $n = 1$ for an ideal SBJ.

Another set of voltage sweeps from –200 mV to +200 mV in 5 mV steps was performed at temperatures from 20 °C to 120 °C, and I_{sat} and n were determined by fitting the

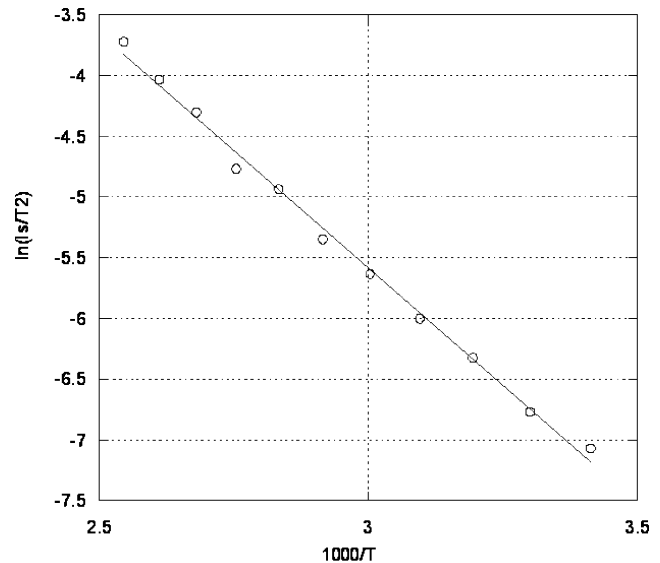


Figure 4. Extraction of the Schottky barrier height by a linear fit of the $\ln(I_{\text{sat}}/T^2)$ versus $1/T$ plot. The slope of the linear fit is used to extract the barrier height.

above experimentally determined I – V data to eq 3, yielding average values of 0.75 nA (at 20 °C) and 1.3, respectively. Using eq 2, a plot of $\ln(I_{\text{sat}}/T^2)$ versus $1/T$ was constructed (Figure 4). The slope of the plotted data was used to extract ϕ_b , yielding an average value of $\phi_b = 0.3$ V.

The Schottky barrier junction could exist at three potential locations: (1) within the fiber, (2) at the fiber–substrate interface, and (3) at the fiber–upper electrode interface (refer to Figure 1f). The nickel particle at the nanofiber tip seemed to have no influence on the device behavior. The VACNF has been shown to behave as a metallic conductor of electrons with properties similar to graphitic fibers,^{14–16} making the prospect of an SBJ within the VACNF unlikely. Based on the electronic similarity of VACNF to graphitic fibers, a value of the work function, ϕ_m , of 4.4 eV was assumed. Metals with values of ϕ_m ranging from 4.3 (Ti) to 5.1 (Ni) were used for the upper interconnect and had no effect on the I – V behavior. These observations suggest that the junction resides at the fiber–substrate interface.

Given $\phi_b = 0.3$ eV as determined above and neglecting barrier contributions of interface states, an electron affinity, χ , of 4.1 eV for the semiconducting material between the nanofiber and the Si is obtained using the relation $\phi_b = \phi_m - \chi$. This value agrees well with published values of χ for SiC.¹⁷

Depth-resolved Auger electron spectroscopy (AES) performed by Teo and co-workers showed that a layer of Si-, C-, and N-containing material is formed on the surface of Si substrates during PECVD growth of VACNF.¹⁸ However, no detailed analysis of the area beneath the VACNF has been reported to date. We performed AES depth profiling to analyze the chemical composition at the fiber–substrate interface. In this experiment, we used an array of carbon nanofibers spaced 5 μm apart on a square grid pattern grown from larger catalyst particles (500 nm diameter). The synthesis was performed in conditions essentially the same as those used for the devices discussed above. We first broke

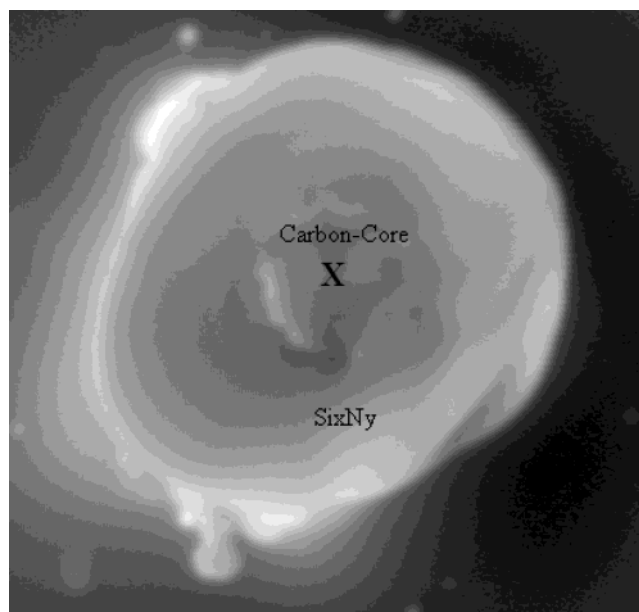


Figure 5. SEM image of the nanofiber stump as used in the following AES analysis, showing an inner carbon core surrounded by a large Si_xN_y sheath.

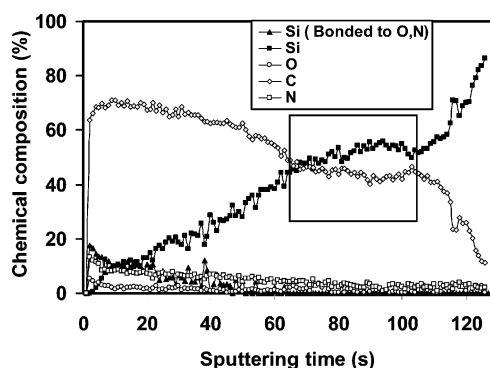


Figure 6. Chemical compositions of C, Si, N, O at the carbon core by the AES as a function of sputtering time. The region in the box was the interface between fiber and substrate, consisting only of silicon and carbon.

the nanofibers near the base using a razor blade, leaving some nanofiber stumps slightly above the substrate (Figure 5). This image clearly shows the inner carbon core surrounded by the outer sheath of Si_xN_y¹⁹ as was determined by initial elemental mapping using AES. We recorded the chemical composition of the core while performing Ar ion sputtering at fixed angles. The atomic concentrations determined from AES elemental signatures in the area of the carbon core (indicated in Figure 5 by an X) have been plotted in Figure 6 as a function of sputtering time. The sputtering rate of the argon ion beam was $\sim 175 \text{ \AA}/\text{min}$, as determined using a calibrated standard SiO₂ sample. The decreasing concentration of carbon and increasing concentration of silicon with sputtering time indicates the diffusion of Si into the base of carbon nanofiber, until both reach approximately 50%, which corresponds to a silicon carbide layer at the nanofiber base. This area is indicated by a square in Figure 6. The layer of SiC is followed by the C-free Si of the substrate.

Our results are consistent with recent work published by Li, et al.¹⁵ where VACNF-based vertical interconnects were fabricated using a process similar to the one presented here. However, the choice of substrates was significantly different. Li et al. used Si wafers coated with a film stack of 500 nm of SiO₂ (lower) and 200 nm of Cr (upper). The devices produced on these substrates did not show any evidence of rectifying behavior and displayed linear *I*–*V* characteristics. The presence of the relatively thick SiO₂ and Cr layers in Li's work would likely block the formation of a semiconducting layer beneath the VACNF.

In conclusion, we have successfully synthesized vertically integrated nanoelectronic devices based on VACNF–SiC Schottky barriers. Our results can be explained using the thermionic model of charge transport across Schottky barrier junctions and suggest that this junction is present at the base of the fiber at the fiber–substrate interface. Unlike other nanodiode fabrication procedures, whose yield is very low and unpredictable, our process is simple and the yield is almost 100 percent for homogeneous fiber height distributions. This architecture may provide a useful tool for creating vertically integrated active nanoelectronic devices with reproducible electrical properties.

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