Initial lithography results from the digital electrostatic e-beam array lithography concept

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The Digital Electrostatically focused e-beam Array direct-write Lithography (DEAL) concept is currently under development at Oak Ridge National Laboratory (ORNL). This concept incorporates a digitally addressable field-emission array (DAFEA) built into a logic and control integrated circuit to function as the write head for an e-beam lithography tool. The electrostatic focusing is integrated on the DAFEA and consists of additional grids lithographically aligned above the emitters and extraction grid, each separated by a dielectric (nominally low-temperature SiO_2) layer. Prototypes of the DAFEA have been fabricated and used to test the focusing of the electron beams and to pattern lines in PMMA resist. First lithography tests have used electron energies of 500 eV to pattern lines less than 1 μm wide at a working distance of 500 μm which extrapolates to $<$300 nm at the nominal DEAL design working distance of 100 μm. Aspects of the DEAL lithography testing and further development are discussed. © *2004 American Vacuum Society.* [DOI: 10.1116/1.1824060]

I. INTRODUCTION

The DEAL lithography concept is a new system configuration in which multiplexed primary sources illuminate the wafer through the use of a simple electrostatic focusing system.[1] The system employs a large array of independently modulated beamlets which allows a raster scan system to be used that has the advantage of being maskless. The key element of this configuration is a nanoscale field emitter electron source currently under development at ORNL.

Prototype DEAL field emission sources have been fabricated and tested at ORNL using vertically aligned carbon nanofibers[2,3] as the field emitter. A typical prototype source device is shown schematically with dimensions and imaged with a SEM in Fig. 1. The devices are fabricated using a self-aligned process for the extraction gate opening while the focus grid opening is defined lithographically.[4] 3×3 arrays of these devices have been fabricated using standard semiconductor fabrication techniques and are mounted on a circuit board with wire bonding to make external electrical connections (Fig. 2). Field emission tests of the completed devices were carried out in a vacuum chamber with a phosphor anode and have shown that the emission follows Fowler–Nordheim characteristics and less than 1% of the emitter current is collected by the extraction and focus grids in well aligned devices.[5]

Current research on DEAL has focused on achieving a proof of lithography demonstration with a path toward development of a prototype lithography system. A developmental test stand has been assembled to demonstrate resist patterning with prototype DEAL sources on PMMA coated glass substrates. In the following section we describe the characteristics of the prototype DEAL sources. Then in Sec. III we present a description of the lithography testbed used in these experiments. In Sec. IV the experimental results from the initial lithography tests are described. Finally, in Sec. V we discuss the present development of the concept and future planned work.

II. PROTOTYPE ELECTRON SOURCE CHARACTERISTICS

The prototype DEAL electron sources use a cold-cathode material related to the carbon nanotube known as a carbon nanofiber that has been deterministically grown in vertically aligned arrays.[2,3] The vertically aligned carbon nanofibers (VACNFs) possess the high geometric field enhancement of the carbon nanotube and small size suitable for massively parallel arrays. This coupled with the ability to deterministically grow the VACNF with a plasma enhanced chemical vapor deposition process on a silicon wafer make it an attractive material to use as the cold-cathode emitters for the DEAL concept.

The electron sources used in this work consist of a triode structure fabricated by using standard semiconductor processing techniques that have been detailed by Guillorn *et al.*[4,5] The emitters are grown on the wafer as the first step and are typically 1 μm tall with a tip radius of 15 nm. The gate and focus electrodes are 150-nm thick layers of Mo with 1-μm-thick SiO_2 layers deposited between the electrodes. The voltage standoff between the electrodes has been measured to be greater than 180 V for the devices used in this study. Typical operating voltages are ~80 V between the gate and cathode to extract electrons at currents of a few nA and the focus electrode operates a few volts above the cathode potential for optimal focus of the beam. The sensitivity of the beam diameter at the collector to focus voltage varia-

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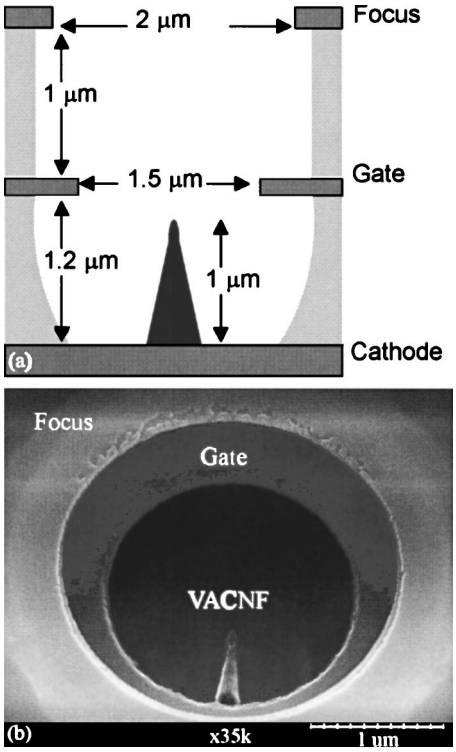

FIG. 1. Schematic diagram of the prototype DEAL device with a SEM micrograph of a device taken at 35° from normal. The vertically aligned carbon nanofiber (VACNF) emitter is seen in the center of the device well.

tions has been modeled for these devices and at a working distance of 100 μm is shown to be nearly 200 nm/V.[6]

III. LITHOGRAPHY TESTBED

A JEOL 5D-II was obtained and modified to use as a DEAL lithography testbed. The electron column of the 5D-II was removed and in its place a spool piece was installed that contains a leveling ring and a bracket attached to a vertical motorized stage to hold the test array chip and position it above the test sample, which is held in the 5D-II cassette. The vertical position control stage is a National Aperture,

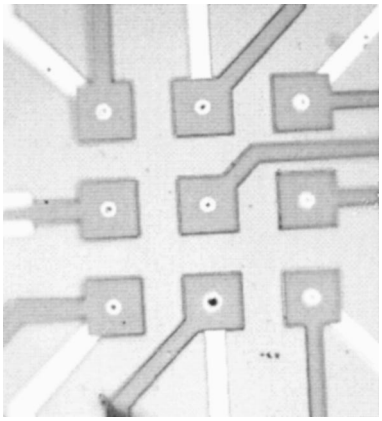

FIG. 2. SEM micrograph of a 3×3 DEAL prototype array showing the electrical connections for the focus grid (dark) and connection to the extraction grid (light).

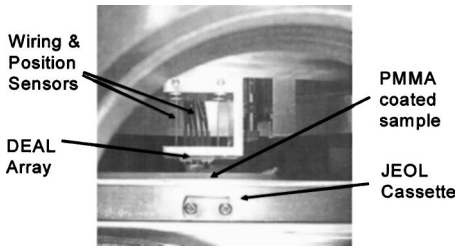

FIG. 3. Picture of the DEAL lithography testbed showing the DEAL array holder mounted above a test sample.

Inc. model MM_3MF with 25 mm travel. The position of the array chip above the test wafer is measured by 4 fiberoptic displacement sensors built into the array holder that are manufactured by Philtec with dual channel reflectance compensation and have 20 nm resolution over a range of 1.3 mm. A picture of the bracket holding a test array chip in the DEAL lithography testbed with the electrical connections and fiber optic position sensors identified is shown in Fig. 3. Keithley 237 source measure units (SMUs) are used to control the voltages on the source devices and monitor the currents from the emitter and currents to the extraction and focus grids.

IV. FOCUSING AND LITHOGRAPHY RESULTS

Tests were performed in the DEAL testbed to pattern lines on PMMA coated glass substrates loaded onto the 5D-II cassette. PMMA was chosen as the resist for these tests because of its well known characterization at the low e-beam energies being used.[7] The prototype array was positioned over the substrate with the vertical stage to a known height above the substrate, typically 500 μm. The cassette was then moved in 5 mm increments at constant speed while the emitter source was operated with the SMUs. The cathode was operated at −500 V with respect to the substrate, which was grounded leading to 500 eV electrons impinging on the PMMA. Typical lines obtained under these conditions in the PMMA from a single emitter after processing are shown in microscope images in Fig. 4. Linewidth variations in this example are due to changes in the focus grid voltage. The variations in linewidth were measured as a function of the focus grid voltage and are in qualitatively good agreement with device modeling. Linewidths of <1 μm have been obtained at this working distance, which extrapolates to <300 nm linewidths for a 100 μm working distance. Finer line sizes of <50 nm are possible from modeling[6] of ideally aligned emitter sources. Voltage adjustments on the focus grid of a few tens of mV are necessary to reach an optimal focus. A planned focus diagnostic will make *in situ* focus voltage settings possible in order to better minimize the feature sizes.

The initial lithography experiments in the DEAL testbed were performed in modest vacuum conditions of 10^{-6} Torr operating pressure. The longevity of emitter sources in this environment was found to be far lower than previously observed in field emission tests on VACNFs.[8] Purging and modifications of the testbed vacuum system were performed

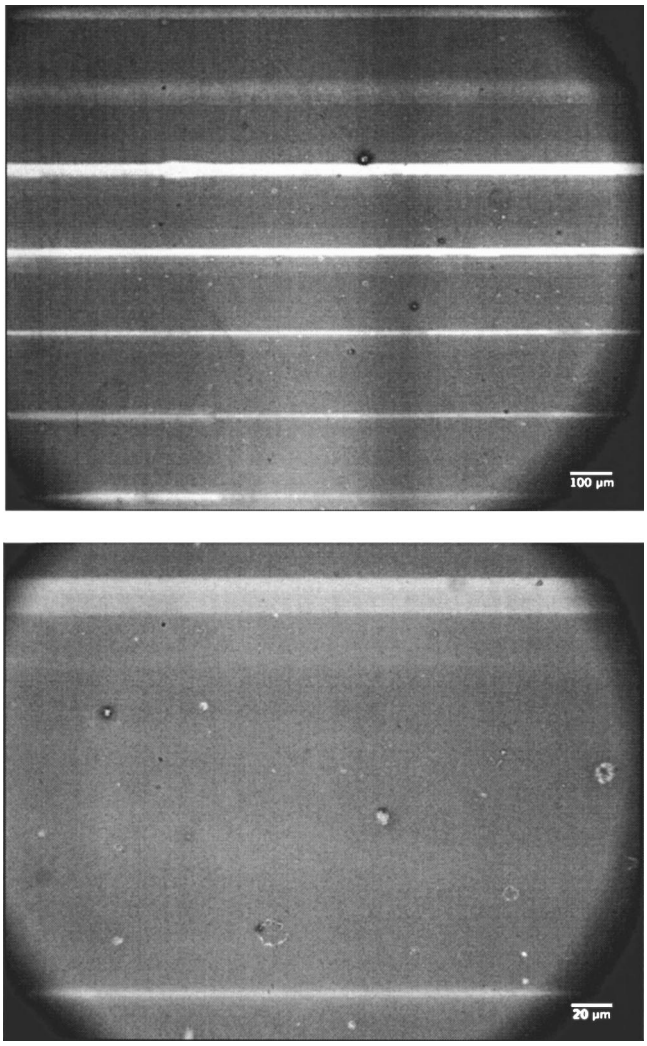

FIG. 4. Microscope images of lines patterned in PMMA from a DEAL source.

and the pressure of high *Z* molecules (presumably hydrocarbons from previous pump oil contamination) was reduced by nearly 2 orders of magnitude. The emitter source lifetime was greatly increased in this improved testbed environment. Tests to measure the emitter source lifetime when operating with different resists are planned.

V. FURTHER DEVELOPMENT OF DEAL COMPONENTS

In addition to the field emitter sources discussed above, the dose control circuit (DCC) and electrostatic lens design are under further development leading toward a full lithography system demonstration. The DCC is designed to control the dose of electrons that reach the wafer from the field emitter sources and is necessary to insure that the dose is equivalent to each pixel. An integrator sums the number of electrons that leave the VACNF and this current is converted to a voltage, which is fed to a comparator that uses an adjustable reference voltage to stop the integration and generate a control signal for the VACNF extraction gate. A board-level DCC has been built and tested for 1 nA currents and achieved an integration time of ~2 ms. A fully integrated CMOS version of the DCC was then fabricated using a 0.5 μm process. This circuit has a complete on-chip system for counting VACNF electrons, including reference voltage generation. The CMOS DCC has achieved integration for currents from 2 to 10 nA. Further work to minimize parasitic capacitance to reduce the integration time for <10 nA is underway.

A focus diagnostic has been designed and is under construction for the lithography testbed that will allow detailed *in situ* measurements of the electron beam spot size. A line pattern on test wafers coupled to an external high resolution current meter (Keithley 428 current amplifier) will provide a measure of the electron beam spot size in two dimensions. This diagnostic will be used before patterning wafers in order to verify the focus voltages on the source device to minimize the feature size.

The optical design of the DEAL sources has been studied recently using the Lorentz 2D and 3D electron trajectory codes from Integrated Engineering Software. An investigation of the depth of focus has revealed that thicker gate and focus electrodes can lead to a smaller spot size and a deeper depth of focus[6] than the present prototype devices which were fabricated by electron beam evaporation of Mo and only had a thickness of 100 nm to 200 nm.[5] Thicker polysilicon electrodes can be deposited by low-pressure chemical vapor deposition (LPCVD) which is planned for our future device processing. This will lead to nearly twice the depth of focus and is anticipated to be less prone to failures from delamination of the gate material, which has been observed with some of the Mo electrodes.

Our initial lithography experiments have been performed using PMMA as the resist which is known to be a fairly strong outgassing material when subjected to electron beams. In order to minimize the possibility of DEAL sources being affected by condensation of outgassing constituents on the emitter surface we are planning to measure the outgassing of different resists under DEAL operating conditions and verify emitter compatibility with different resists at a close working distance. Others have studied outgassing from resists for EUV applications,[9–12] but little data exists for low-energy e-beam applications.

VI. CONCLUSIONS

The DEAL concept is under development to lead to a highly parallel lithography system that can potentially pattern semiconductor wafers at high-throughput rates without the use of a mask. Initial lithography has been accomplished with DEAL electron sources by patterning lines less than 1 μm wide in PMMA at a 500 μm working distance, which extrapolates to <300 nm at the nominal DEAL design working distance of 100 μm. Further improvements in source alignment and improved focusing with thicker gate materials are under development to lead to smaller feature sizes and continued progress toward a working prototype lithography system.

ACKNOWLEDGMENTS

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